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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GENCO, BRIAN C	
ART UNIT	PAPER NUMBER
2615	

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13

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/322,321	MORRIS ET AL.	
	Examiner	Art Unit	
	Brian C Genco	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 23-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 23-30 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Applicant's arguments filed January 7, 2004 have been fully considered by the Examiner but are not deemed persuasive.

Applicant argued that shift register R1 of the Berger reference is not coupled to control a reset of sensor elements, but rather to carry out reading of each line and is therefore different than the reset of a sensor element by a reset shift register as recited in claim 23.

In response, Examiner notes that means 4 is a reset shift register in that as disclosed on column 3, lines 14-17 and column 4, lines 52-60 charges are read out to a drain. Examiner notes that this constitutes a reset of sensor elements of a line.

Applicant argued that Examiner ignored the limitation that the reset sift register is feed a pair of reset bits.

In response, Examiner notes page 4, line 15-18 of Paper No. 11. Examiner notes in particular the reference to begin an integration time by resetting pixels as disclosed in Berger in Fig. 3 through the showing of the Period R before Period S. Suzuki further describes when providing different integration times for the different colors all of the colors are reset at the same time t0 as shown in Fig. 3 so as to begin the integration period for each color. Examiner notes that Suzuki discloses the use of photodiodes. Fossum teaches to provide a reset so as to perform CDS wherein Fossum discloses that in providing a CDS for a photodiode the reset should take place at the end of the integration period as shown in Fig. 4B and described in paragraph 0049. As such, in combining the teachings of the three references as a whole on of ordinary skill in the

art would clearly recognize to provide two reset bits, one to start the integration period and one to perform CDS.

Applicant argues that the combination of references does not teach to operate the shift registers so that the reset bits and the read bit shift through their respective registers while an image frame is being captured with one of the reset bits of the pair always being one or more rows ahead of the read bit to mark the start of integration, and the other one of the pair to generate a correlated double sampling pixel reset value.

In response, Examiner notes the teaching of Berger wherein it is disclosed to be able to vary the integration time of different lines by resetting a line at one time and later reading that line one or more line display intervals later (column 3, lines 9-12; column 5, lines 14-18; lines 28-39; Fig. 2). Therefore in combining all of the references as a whole Berger teaches to provide a first reset operation so as to start an integration period and a read operation so as to end integration and read out the generated image signals one or more lines after the first reset operation. Fossum teaches to then generate a second reset bit at the end of the integration period so as to perform CDS. Suzuki teaches to perform these operations independently to different colors through the use of different hardware, namely in this case to provide a reset shift register and wordline shift register for each color so as to enable the variation of exposure time for each color and each line, thus extending the dynamic range of the image sensor and enabling the variation of the integration time to a considerable extent.

Applicant argues that Fossum does not teach a "reset bit" but rather merely an operation during correlated double sampling.

In response, Examiner notes that there is inherently some sort of control logic associated with the Fossum circuit structure so as to apply the control signals to the various transistors and enable the Fossum circuit to work in its intended purpose. Examiner further notes that Berger discloses control logic necessary to perform the reset operation disclosed by Fossum through the use of a reset shift register, element 4 of Fig. 1. As such, Fossum does not need to disclose a "reset bit" since it is already taught by Berger and further since it is an implicit feature of the Fossum reference to apply a "reset bit" to the reset transistor 106 so as to perform the described reset operation. Examiner further notes Figs. 4A and 4B where it appears that there is clearly some sort of "reset bit" disclosed in waveform RST.

Applicant argues that Fossum does not disclose resetting at the end of integration.

In response, Examiner directs Applicant to Fig. 4B and paragraph 0049 wherein when using photodiodes the reset bit occurs at the end of the integration period. Examiner notes that Berger discloses the use of photodiodes on column 5, lines 45-56 and further Suzuki discloses the use of photodiodes.

Applicant argues that the Examiner has ignored how one of ordinary skill in the art would modify the Berger or Fossum sensors into one that detects color, using the particular reset and wordline shift register logic recited in claim 23.

In response, see Examiner's answers to the arguments above and the rejection previously presented.

As Applicant has not amended any of the claims and all of Applicant's arguments have been answered above, the previous grounds of rejection still stand.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 23-25 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 4,609,825 to Berger et al.) in view of (US PG-PUB 2003/0193597 to Fossum et al.) in further view of (USPN 4,709,259 to Suzuki).

In regards to claim 23 Berger et al., herein Berger discloses an integrated circuit comprising:

a pixel array (e.g., see Fig. 1);

a first reset shift register having a plurality of outputs, each output being coupled to control a reset of sensor elements that are in a respective one of the rows of the array (e.g., element 4 of Fig. 1);

a wordline shift register having a plurality of outputs, each output being coupled to control a readout of the sensor elements that are in a respective one of the rows of the array (e.g., element 5 of Fig. 1);

control logic coupled to feed (a) the first shift register with a reset bit and (b) the wordline shift register with a read bit, and to operate the reset and wordline shift registers so that the reset bit and the read bit shift through their respective registers while an image frame is being captured, with the reset bit always being one or more rows ahead of the read bit to mark the start of integration, wherein the control logic is to program the reset bit and the read bit to set the integration time independently for different lines (e.g., column 4, lines 24-30 and 52-60; column 5, lines 14-27; Fig. 2).

Berger does not disclose that the reset bit is used for generating a correlated double sampling (CDS) reset value. In contrast, Berger discloses draining the reset charges (column 4, lines 24-30 and 52-60). It is extremely well known in the art to use the reset bit in order to generate a CDS reset value as taught by Fossum et al. Fossum et al., herein Fossum, discloses sampling a reset voltage at the end of integration in order to reduce various noise introduced into the signals (paragraphs 0028, 0029, and 0033).

Neither Berger nor Fossum disclose a color sensor array having a plurality of sensor elements of different first and second colors, arranged in rows and columns, wherein the first reset shift register is used to control the integration time of the first color and a second reset shift register is used to control the integration time of the second color.

Suzuki discloses a color image sensor wherein the integration time for each color is adjustable so as to increase the dynamic range of the sensor (column 2, lines 17-21). This is accomplished by having separate registers for each color so as to reset all of the colors at the same time to start the integration period and to read out the colors at their respective integration times as depicted in Fig. 3 (e.g., column 4, lines 6-41; column 5, line 27 – column 6, line 16);

Figs. 1-3). Therefore it would have been obvious to have had separate reset shift registers for each color so as to enable variable exposure times not only on different lines but on different colors as well thereby increasing the dynamic range of the sensor. As such, for at least the red and green colors two reset bits would be needed, one to mark the start of integration as taught by both Berger and Suzuki and the other to perform CDS at the end of the integration period as taught by Fossum.

In regards to claim 24 see Fig. 1 of Suzuki.

In regards to claim 25 see examines notes on the above rejections. Note that the combined teaching of Berger and Suzuki teach to have a reset shift register for each color. Note further that Suzuki discloses using the Bayer color filter wherein all three colors are present on any one given line. As such, one of ordinary skill in the art would recognize that three reset metal lines would be used for each row. As such there are two reset metal lines for each row.

In regards to claims 27-29 see examines notes on the above rejections.

Claims 26 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 4,609,825 to Berger et al.) in view of (US PG-PUB 2003/0193597 to Fossum et al.) in further view of (USPN 4,709,259 to Suzuki) in further view of (USPN 5,541,645 to Davis).

In regards to claims 26 and 30 see Examiners notes on the rejections above. Examiner notes that it is known in the art that in conventional lighting the blue color typically has the lowest intensity thus has the longest integration time. Davis discloses that since this is the case, in order to have a time efficient image sensor, and minimize dead time one would only want to reset the blue color once (e.g., column 5, line 26 – column 6, line 7). Therefore it would have

been obvious to one of ordinary skill in the art at the time of the invention to have only had one reset for the blue reset register, or third reset register, in order to minimize dead time and thus have a time efficient image sensor.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian C. Genco who can be reached by phone at 703-305-7881 or by fax at 703-746-8325. The examiner can normally be reached on Monday thru Thursday 7:30am to 4:30 pm and every other Friday 7:30am to 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on 703-308-9644. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the customer service office whose telephone number is 703-308-4357.

Brian C Genco
Examiner
Art Unit 2615

February 23, 2004

ANDREW CHRISTENSEN
SUPERVISORY PATENT EXAMINER
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